

Seat No. : \_\_\_\_\_

**DA-101**

**December-2018**

**B.C.A., Sem.-III**

**CC-201 : Computer Organization and Advanced Microprocessor  
(Old Course)**

**Time : 2:30 Hours]**

**[Max. Marks : 70**

- Instructions :**
- (1) Begin new answer on a new page.
  - (2) Draw diagrams wherever necessary.
  - (3) Figures to the right indicate full marks.

1. (A) Answer the following :

- (i) Explain instruction format with example. 7
- (ii) Write a note on interrupts and its types. 7

**OR**

- (i) Explain Von Neumann Architecture with block diagram.
- (ii) Write a note on bus with its usage.

(B) Attempt any **four** out of **six** : 4

- (i) The ratio of pulse width to time period is called \_\_\_\_\_.
- (ii) In IEEE representation of single precision floating point number, mantissa is of \_\_\_\_\_ bits.
- (iii) \_\_\_\_\_ bit is used to represent negative sign in signed magnitude form.
- (iv) \_\_\_\_\_ stores the result of the last processing step of the ALU.
- (v) 11000-10000 using 1's complement is \_\_\_\_\_.
- (vi) The CPU states can be divided into two: \_\_\_\_\_ and Running.

2. (A) Answer the following :

- (i) Define Encoder. Write a note on Decimal-to-BCD Encoder. 7
- (ii) Draw logic circuit and truth table of JK flip-flop. 7

**OR**

- (i) Define Multiplexer. Explain 4X1 MUX with appropriate diagrams.
- (ii) Draw schematic diagram and truth table of full adder.

(B) Attempt any **four** out of **six** : 4

- (i) \_\_\_\_\_ is two-state device which offers basic memory cell for sequential logic operations.
- (ii) In half adder, the carry output is a simple \_\_\_\_\_ function and the sum is an exclusive-OR function.
- (iii) A \_\_\_\_\_ is a device which essentially performs the opposite operation to the multiplexer.
- (iv) \_\_\_\_\_ and \_\_\_\_\_ gates are called universal gates.
- (v) Octal-to-Binary encoder takes \_\_\_\_\_ inputs and gives \_\_\_\_\_ outputs.
- (vi) \_\_\_\_\_ flip-flop acts as a toggle switch.

3. (A) Answer the following :

- (i) Write a note on associative memory. 7
- (ii) What is mapping ? Write a note on direct mapping in cache memory. 7

**OR**

- (i) Write a note on cache coherence with its solution.
- (ii) Discuss various parameters to choose a memory.

(B) Attempt any **three** out of **five** : 3

- (i) The performance of the cache is measured in terms of \_\_\_\_\_ ratio.
- (ii) Cycle time ( $T_c$ ) = \_\_\_\_\_ + Recovery Time ( $T_r$ ).
- (iii) Magnetic tape is an example of \_\_\_\_\_ access memory.
- (iv) \_\_\_\_\_ is the access time taken by the first access in a series of accesses.
- (v) \_\_\_\_\_ algorithm chooses the block frame that has been referenced by the CPU very less number of times from the time it was mapped onto the cache memory.

4. (A) Answer the following :

- (i) Write a note on functional unit of 8086. 7
- (ii) Compare CISC and RISC processors. 7

**OR**

- (i) Classify and explain various addressing modes of 8086.
- (ii) Discuss mobile and tablet processors.

(B) Attempt any **three** out of **five** :

**3**

- (i) A \_\_\_\_\_ processor allows instruction level parallelism within a single processor.
  - (ii) In \_\_\_\_\_ addressing mode, operand is a part of the instruction.
  - (iii) \_\_\_\_\_ address determines how far is the memory location from the starting address of the segment register.
  - (iv) A \_\_\_\_\_ is a digital computer built on a single chip used to control application.
  - (v) Intel 8086 is a \_\_\_\_\_ bit microprocessor that operates in two modes - minimum mode and maximum mode.
- \_\_\_\_\_

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B.C.A., Sem.-III

## CC-201 : Computer Organization (New Course)

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- Instructions :**
- (1) Begin new answer on a new page.
  - (2) Draw diagrams wherever necessary.
  - (3) Figures to the right indicate full marks.

1. (A) Answer the following :

- (i) Write a note on 4-bit synchronous binary counter. 7
- (ii) Explain half-adder circuit with logic diagram. Also show the use of half-adder modules to construct NAND and NOR gates. 7

**OR**

- (i) Explain 2-to-4 line decoder with NAND gates.
- (ii) Define register. Explain 4-bit register with parallel load.

(B) Attempt any **four** out of **six** : 4

- (i) The output of \_\_\_\_\_ gate is 1 if any input is 1 but excludes the combination when both inputs are 1.
  - (a) XOR (b) XNOR
  - (c) NAND (d) NOR
- (ii) In SR flip-flop, if S=1 and R=0 when C (CLK) changes from 0 to 1, output Q is set to \_\_\_\_\_.
  - (a) 0 (b) 1
  - (c) No change (d) Indeterminate
- (iii) The \_\_\_\_\_ family provides the highest-speed digital circuits in integrated form which is used in systems such as supercomputers and signal processors where high speed is essential.
  - (a) TTL (b) ECL
  - (c) CMOS (d) DTL

- (iv) A \_\_\_\_\_ is a group of flip-flops with each flip-flop capable of storing one bit of information.
- (a) Encoder (b) Decoder  
(c) Multiplexer (d) Register
- (v) Flash memory is a form of \_\_\_\_\_ in which a block of bytes can be erased in a very short duration.
- (a) ROM (b) PROM  
(c) EPROM (d) EEPROM
- (vi) A register capable of shifting its binary information in one or both directions is called a \_\_\_\_\_ register.
- (a) Shift (b) Unidirectional  
(c) Bidirectional (d) Load

2. (A) Answer the following :

- (i) Write a note on 4-bit binary adder-subtractor. 7  
(ii) Explain one stage of arithmetic logic shift unit with function table. 7

**OR**

- (i) Write a note on 4-bit arithmetic circuit with function table.  
(ii) Explain error detection with odd parity bit.

(B) Attempt any **four** out of **six** : 4

- (i) The standard alphanumeric binary code is the \_\_\_\_\_, which uses seven bits to code 128 characters.
- (a) ANSI (b) BCD  
(c) ASCII (d) UNICODE
- (ii) A floating-point number is said to be normalized if the most significant digit of the mantissa is \_\_\_\_\_.  
(a) Non-zero (b) Zero  
(c) Signed (d) Unsigned
- (iii) A three-state gate is a digital circuit that exhibits three states : 0, 1 and \_\_\_\_\_.  
(a) Low-impedance (b) High-impedance  
(c) Medium-impedance (d) None of these

- (iv) The transfer of information from a memory word to the outside environment is called a \_\_\_\_\_ operation.
  - (a) Complement (b) Execute
  - (c) Read (d) Write
- (v) There are three types of shift microoperations for serial transfer of data - logical, circular and \_\_\_\_\_.
  - (a) Left-right (b) Physical
  - (c) Rotate (d) Arithmetic
- (vi) 2's complement of 1010 is \_\_\_\_\_.
  - (a) 0111 (b) 1011
  - (c) 0110 (d) 1110

3. (A) Answer the following :

- (i) Write a note on 16-bit common bus system. 7
- (ii) Explain instruction cycle with flowchart. 7

**OR**

- (i) List out and explain memory-reference instructions.
- (ii) Explain any three addressing modes with the help of an appropriate numerical example.

(B) Attempt any **three** out of **five** : 3

- (i) Bit Z (zero) is set to \_\_\_\_\_ if the output of the ALU contains all 0's.
  - (a) Zero (b) 1
  - (c) -1 (d) 0
- (ii) In the \_\_\_\_\_ organization, the control logic is implemented with gates, flip-flops, decoders and other digital circuits.
  - (a) Hardwired control (b) Microprogrammed control
  - (c) Control memory (d) None of these
- (iii) When IEN is \_\_\_\_\_, the flags can not interrupt the computer.
  - (a) 0 (b) 1
  - (c) ION (d) None of these
- (iv) Non-embedded computer architectures are basically \_\_\_\_\_ architectures in which programs and data reside in the same memory system.
  - (a) RISC (b) SPC
  - (c) CISC (d) DSP
- (v) The mode bit - I is \_\_\_\_\_ for a direct address and \_\_\_\_\_ for an indirect address.
  - (a) 0, 0 (b) 1, 0
  - (c) 0, 1 (d) 1, 1

4. (A) Answer the following :
- (i) Explain source-initiated and destination-initiated transfer using handshaking. 7
  - (ii) Explain associative memory with block diagram. 7

**OR**

- (i) Explain DMA with block diagram of DMA controller.
  - (ii) Explain any one type of mapping procedure in organization of cache memory with an appropriate example.
- (B) Attempt any **three** out of **five** : 3
- (i) The average time required to reach a storage location in memory and obtain its contents is called the \_\_\_\_\_ time.
    - (a) Seek (b) Access
    - (c) Mean (d) None of these
  - (ii) \_\_\_\_\_ allows the DMA controller to transfer one data word at a time, after which it must return control of the buses to the CPU.
    - (a) Burst transfer (b) Cycle stealing
    - (c) Priority encoder (d) Daisy-chaining priority
  - (iii) The performance of cache memory is frequently measured in terms of a quantity called \_\_\_\_\_ ratio.
    - (a) Heat (b) High
    - (c) Low (d) Hit
  - (iv) Input output devices attached to the computer are also called
    - (a) Peripherals (b) Read-Write
    - (c) Workspace (d) None of these
  - (v) In the \_\_\_\_\_ configuration, the CPU has distinct input and output instructions, and each of these instructions is associated with the address of an interface register.
    - (a) Memory-Mapped I/O (b) Isolated I/O
    - (c) Both (d) None of these

